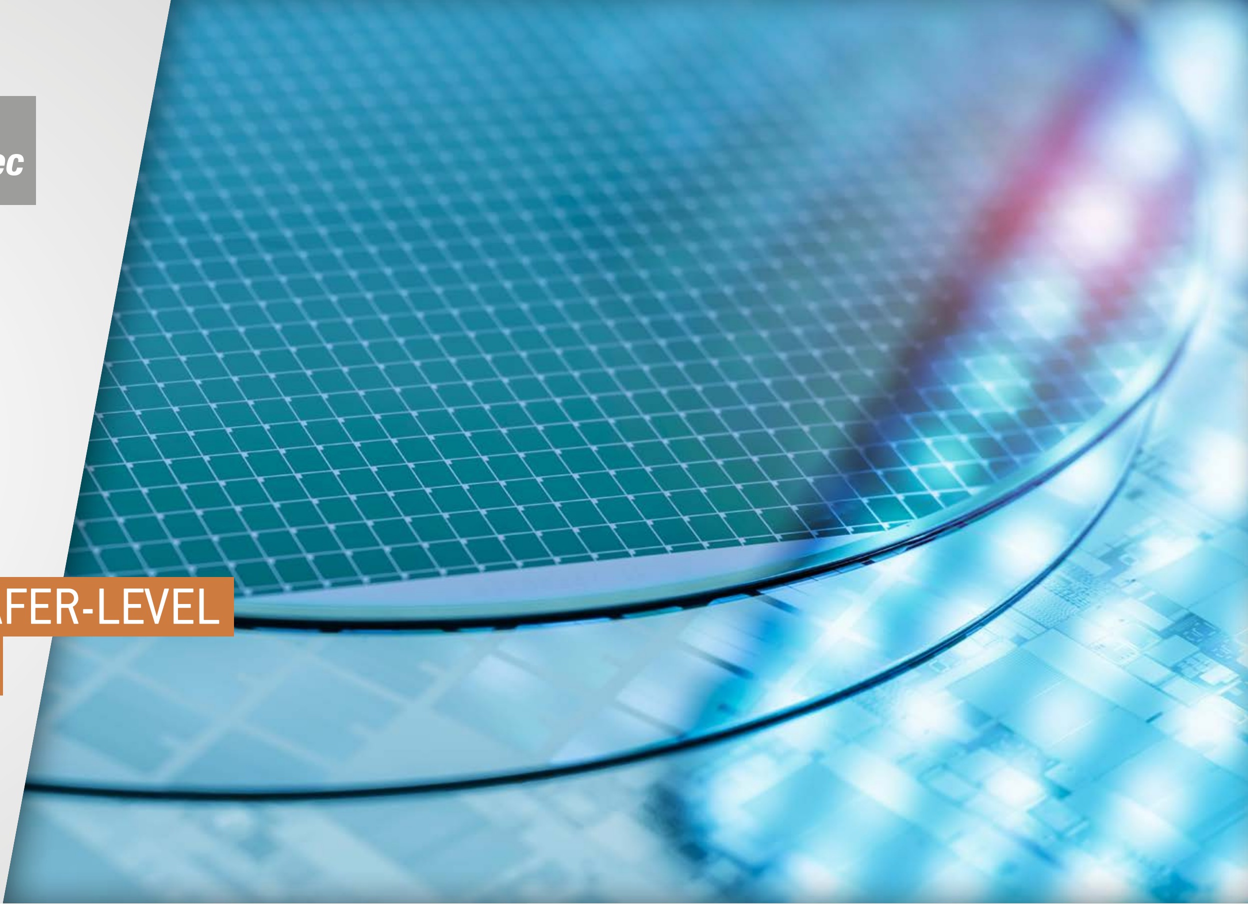
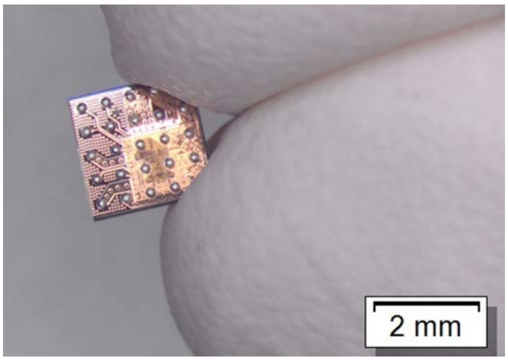


FAN OUT WAFER-LEVEL PACKAGING

FOWLP - A SOLUTION FOR MINIATURIZED PACKAGES

Fan-Out Wafer-Level Packaging (FOWLP) is an advanced semiconductor packaging technology that enables higher performance, greater integration density, and reduced form factor compared to traditional packaging methods. It plays a critical role in the miniaturization and functionality of modern electronic devices.

- Heterogeneous Integration
- Excellent RF and thermal performance
- SMT solderable
- High integration density
- Substrate-less



FAN OUT WAFER-LEVEL PACKAGING - UNIQUELY AVAILABLE IN EUROPE IN SMALL AND MEDIUM VOLUMES

Incoming Wafer Test & Dicing ▸ High accuracy Die Bonding ▸ Compression Molding ▸ RDL ▸ Solder Ball Attach ▸ Laser Marking ▸ Dicing ▸ Final Test

■ AEMtec in-house processes
■ External processes

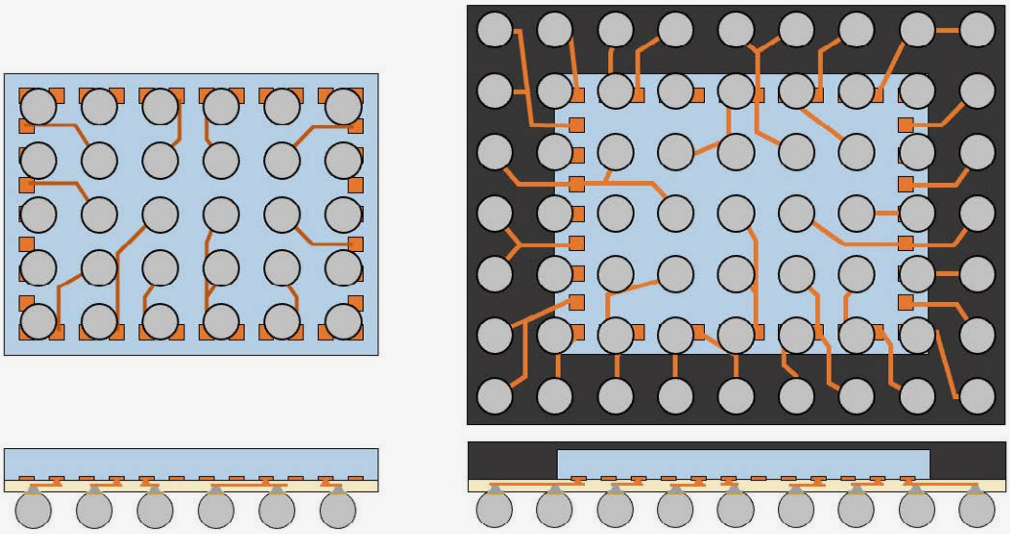
Small and medium production volumes of FOWLP are largely inaccessible in Europe due to high entry costs and limited availability. AEMtec fills this critical gap. FOWLP solutions tailored specifically for low- to mid-volume production needs.

FOWLP IS A SOLUTION FOR MINIATURIZED PACKAGES WITH EXCELLENT **RF** AND **THERMAL** PERFORMANCE.

Unlike **Fan-In Wafer-Level Packaging (WLP)**, where interconnects are confined within the original footprint of the die, FOWLP “fans out” the connections beyond the die area.

This is achieved by embedding the die in a reconstituted wafer using a molding compound, allowing more space for additional redistribution layers (RDLs). These RDLs facilitate external connections, enabling the integration of multiple components (such as analog and digital dies) within a single package.

Depending on the application, FOWLP technology can offer key advantages over traditional Flip Chip packaging.



Fan In
Pads and RDL traces are routed within the Die area

Fan Out
Pads and RDL traces are routed within and beyond the Die area

Conceptual comparison: Fan-In vs Fan-Out Wafer Level Packaging

AEMtec GmbH
James-Franck- Str. 10
12489 Berlin
Germany

Phone: +49 30 6392 7300
Fax: +49 30 6392 7302
Email: info@AEMtec.com
Web: www.AEMtec.com
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TO OUR FOLDERS